WHAT IS CLAIMED IS:

1. A lateral transistor comprising:

a semiconductor substrate of the first conductivity type;

a buried region of the second conductivity type disposed on said semiconductor substrate;

a uniform base region of the second conductivity type disposed on said first buried region;

a plug region of the second conductivity type disposed in said uniform base region, the plug region protrudes from a top surface of said uniform base region so as to reach to said buried region;

first and second main electrode regions of the first conductivity type disposed in and at the top surface of said uniform base region; and

a graded base region of the second conductivity type disposed in said uniform base region, enclosing bottom and side of said first main electrode region, the graded base region has a doping profile such that impurity concentration decreases towards said second main electrode region from said first main electrode region,

wherein a combination of said uniform base region and said graded base region serves as a base region.

2. The lateral transistor of claim 1, wherein said second main electrode region is formed in a ring shape, configured such that said second main electrode region surrounds said graded base region.

3. The lateral transistor of claim 2, wherein said second main electrode region is formed in a rectangular ring shape.

4. The lateral transistor of claim 1, further comprising a base contact region disposed in and at a top surface of said plug region.

5. The lateral transistor of claim 2, further comprising a base wiring contacting with said base contact region.

6. A semiconductor integrated circuit including a lateral transistor, the lateral transistor comprising:

a semiconductor substrate of the first conductivity type;

a first buried region of the second conductivity type disposed on said semiconductor substrate;

a uniform base region of the second conductivity type disposed on said first buried region;

a first plug region of the second conductivity type disposed in said uniform base region, the first plug region protrudes from a top surface of said uniform base region so as to reach to said first buried region;

first and second main electrode regions of the first conductivity type disposed in and at the top surface of said uniform base region; and

a graded base region of the second conductivity type disposed in said uniform base region, enclosing bottom and side of said first main electrode region, the graded base region has a doping profile such that impurity concentration decreases towards said second main electrode region from said first main electrode region,

wherein a combination of said uniform base region and said graded base region serves as a first base region of said lateral transistor.

7. The semiconductor integrated circuit of claim 6, further including a vertical transistor, the vertical transistor comprising:

a second buried region of the second conductivity type disposed on said semiconductor substrate, the second buried region serving as a part of a third main electrode region of said vertical transistor;

a drift region of the second conductivity type disposed on said second buried region;

a second base region of the first conductivity type disposed in said drift region; and

a fourth main electrode region of the second conductivity type disposed in said second base region.

8. The semiconductor integrated circuit of claim 7, further comprising a connecting wiring connecting said second main electrode region with second base region.

9. The semiconductor integrated circuit of claim 7, further comprising an element isolation region disposed between said uniform

base region and said drift region.

10. The lateral transistor of claim 7, wherein said second main electrode region is formed in a ring shape, configured such that said second main electrode region surrounds said graded base region.

11. The lateral transistor of claim 10, wherein said second main electrode region is formed in a rectangular ring shape.

12. The lateral transistor of claim 7, further comprising a first base contact region disposed in and at a top surface of said first plug region.

13. The lateral transistor of claim 12, further comprising a first base wiring contacting with said first base contact region.

14. A method of fabricating a semiconductor integrated circuit comprising:

selectively forming a first diffusion region of the second conductivity type on a semiconductor substrate of a first conductivity type;

growing an epitaxial layer of the second conductivity type on said first diffusion region so as to make said first diffusion region a first buried region;

selectively diffusing impurity atoms of the second conductivity type so as to form a first plug region of the second conductivity type, from a top surface of said epitaxial layer such that a bottom of said first plug region reaches to said first buried region;

selectively diffusing impurity atoms of the second conductivity type so as to form a graded base region of the second conductivity type, from the top surface of said epitaxial layer, a lateral position of the graded base region is separated from the lateral position of said first plug region and a vertical position of the graded base region is separated from the vertical position of said first buried region, the graded base region has a doping profile such that impurity concentration decreases towards peripheral region from central region of the graded base region;

forming a first main electrode region of the first conductivity type

in and at the top surface of said graded base region; and

forming a said second main electrode region of the first conductivity type, so as to sandwich said graded base region between said first and second main electrode regions, in and at the top surface of said epitaxial layer.

15. The method of claim 14, further comprising selectively forming a second diffusion region of the second conductivity type on said semiconductor substrate before said growing the epitaxial layer, a lateral position of the second diffusion region is separated from the lateral position of said first diffusion region, wherein said growing the epitaxial layer makes said second diffusion region a second buried region, the second buried region serving as a part of a third main electrode region.

16. The method of claim 15, further comprising forming a second base region of the first conductivity type above said second buried region in the epitaxial layer.

17. The method of claim 16, further comprising forming a fourth main electrode region of the second conductivity type in and at a top surface of the second base region.

18. The method of claim 14, further comprising forming a silicon oxide film on the top surface of said epitaxial layer, wherein impurity atoms for forming said graded base region and said first main electrode region are doped through the same diffusion window formed in said silicon oxide film.

19. The method of claim 14, wherein said selectively diffusing impurity atoms so as to form the graded base region and said forming the first main electrode region in and at the top surface of the graded base region comprises;

said forming the silicon oxide film on the top surface of the epitaxial layer;

forming the diffusion window in the silicon oxide film;

implanting impurity ions of the impurity atoms of the second

conductivity type through the diffusion window;

annealing the semiconductor substrate so as to form the graded base region up to an intermediate diffusion depth of the graded base region ;

implanting impurity ions of the first conductivity type through the diffusion window; and

annealing the semiconductor substrate so as to form the first main electrode region and to drive-in the graded base region deeper than the intermediate diffusion depth.